

ADITYA SODHANI

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Research Interests

Fault-tolerant quantum computing: cryogenic, real-time decoders for quantum error-correcting codes; compilation and synthesis of low-overhead encoder circuits for quantum LDPC codes; machine-learned decoding; VLSI and computer architecture for quantum control.

Education

University of Minnesota, Minneapolis, USA

Ph.D., Electrical and Computer Engineering; Graduate Minor in Mathematics

Jan. 2024 – May 2028 (expected)

GPA: 4.0/4.0

Birla Institute of Technology and Science (BITS), Pilani, India

Master of Engineering, Microelectronics. Gold Medalist, Batch of 2022

Aug. 2020 – June 2022

CGPA: 3.93/4.0

Birla Institute of Technology and Science (BITS), Pilani, India

Bachelor of Engineering, Electrical and Electronics Engineering

Aug. 2016 – June 2020

CGPA: 3.78/4.0

Publications

Journal articles

- [J1] **A. Sodhani**, P. Kumar, S. S. Garani, and K. K. Parhi, “Optimizing encoder circuits of entanglement-assisted quantum LDPC codes via beam search,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2026. doi: [10.1109/TCSII.2026.3734949](https://doi.org/10.1109/TCSII.2026.3734949).
- [J2] **A. Sodhani** and K. K. Parhi, “Encoder circuit optimization for nonbinary quantum error correction codes in prime dimensions: An algorithmic framework,” *IEEE Transactions on Quantum Engineering*, vol. 7, pp. 1–15, 2026. doi: [10.1109/TQE.2026.3669054](https://doi.org/10.1109/TQE.2026.3669054).

Preprints

- [P1] **A. Sodhani** and K. K. Parhi, “Noise-aware synthesis of quantum LDPC encoder circuits via two-sided Hamming descent,” [arXiv:2607.04462](https://arxiv.org/abs/2607.04462), July 2026. Under review.

Research Experience

University of Minnesota

Graduate Research Assistant, VLSI and quantum computing group of Prof. Keshab K. Parhi

Jan. 2024 – present

Minneapolis, MN

- **Cryogenic decoders for quantum error correction.** Designed a fixed-latency, lookup-table surface-code decoder in RTL for operation at 4 K that resolves more than 97% of syndrome rounds locally at practical error rates; synthesized in GlobalFoundries 22 nm with a cryo-CMOS power model giving $12.8 \mu\text{W}$ per $d = 7$ decoder. Monte Carlo benchmarking against minimum-weight perfect matching shows no threshold degradation for $d = 3$ –17. Extended the two-stage approach to IBM’s Bivariate Bicycle $[[144,12,12]]$ qLDPC code (96% of blocks resolved locally, BP+OSD fallback).
- **Low-overhead encoder circuits for quantum LDPC codes.** Developed a two-sided Hamming descent algorithm and a noise- and hardware-aware compilation pipeline (routing, noise-aware selection, live-range scheduling) for CSS LDPC encoders: 53.8% fewer CNOTs in aggregate across 17 codes, up to 71% lower routed two-qubit depth, up to 13.7% lower preparation failure [P1]. Devised a Hamming-guided beam search for entanglement-assisted QC-LDPC encoders, 7.3–34.0% fewer CNOTs than the standard construction on all eight codes tested [J1], and an algorithmic framework for qudit stabilizer-code encoders with up to 44% fewer gates [J2].
- **Learned decoding on experimental data.** Trained a 21K-parameter recurrent-transformer decoder (PyTorch, INT4 quantization-aware training) on Google’s experimental Sycamore distance-3 surface-code data: 5.2% lower logical error rate than minimum-weight perfect matching on 35,000 held-out shots.

Indian Institute of Science (IISc), Bengaluru, India

Research Collaborator (remote), group of Prof. Shayan Srinivasa Garani

Oct. 2024 – present

- Fault-tolerant encoders for quantum LDPC codes: qubits partitioned into contiguous blocks with Bell pairs for transversal operations; probabilistic error-propagation bounds under a depolarizing noise model; demonstrated on an entanglement-assisted code with linear overhead scaling. Co-authored [J1].

Industry Experience

Qualcomm India Pvt. Ltd. <i>Hardware Engineer – RTL Performance Analysis and Verification</i>	Dec. 2021 – Dec. 2023 <i>Bengaluru, India</i>
– Analyzed premier-tier Snapdragon SoC memory-subsystem RTL (memory controller, last-level cache controller) and debugged microarchitectural limitations causing bandwidth loss under various traffic patterns. – Built a Python automation framework linking performance runs of the DDR memory subsystem to results analysis (Verilog, Python, Verdi, Linux).	
Micron Technology <i>Design Verification Engineer – 3D-NAND</i>	May 2020 – Nov. 2020 <i>Hyderabad, India</i>
– Developed a UVM-based testbench for constrained-random verification of a memory controller; owned test vectors for multiple design features, drove coverage closure, and automated parallel test-vector runs and failure post-processing in Python.	
Université de Sherbrooke <i>Research Intern, Mitacs Globalink Research Internship, Ambient Intelligence group</i>	May 2019 – Aug. 2019 <i>Sherbrooke, Canada</i>
– IoT solutions for elderly healthcare: interfaced LoRa modules (Raspberry Pi host) with a Conduit gateway to form a LoRaWAN network; integrated devices, APIs and online services in Node-RED.	

Honors and Awards

DAC Young Fellow, 63rd Design Automation Conference	2026
Best Poster Presentation Award, IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)	2025
CSE Ph.D. Fellowship, College of Science and Engineering, University of Minnesota (one year)	
Gold Medalist, M.E. Microelectronics, BITS Pilani (Batch of 2022)	2022
Mitacs Globalink Research Internship, Canada	2019
Merit Scholarship (80% fee waiver) for all four years of the B.E., BITS Pilani	2016 – 2020
Best Poster Presentation Award, Symposium on Carbon Nanomaterial Electronics, BITS Pilani	

Talks and Posters

“Noise-Aware Quantum LDPC Encoder Synthesis,” poster, DAC Young Fellows Program, 63rd DAC	July 2026
Poster on optimized encoders for quantum error-correcting codes, IEEE MWSCAS 2025 (Best Poster Award)	Aug. 2025

Technical Skills

Quantum software:	Stim, PyMatching, Cirq, Qiskit; BP+OSD; custom lookup-table decoders; stabilizer-tableau simulation
Languages:	Python, C, C++, Rust, Julia, MATLAB, CUDA, Verilog, SystemVerilog, Bash, Tcl
Hardware design:	RTL design, UVM verification, Synopsys Design Compiler, Cadence Genus/Innovus/Xcelium, Synopsys Verdi, Xilinx Vivado, Icarus Verilog, Cadence Virtuoso, SPICE
Machine learning:	PyTorch (quantization-aware training), NumPy, SciPy, Matplotlib

Selected Coursework

Quantum Mechanics; Mathematics of Quantum Computing; Quantum Computing and the Physical Basis of Computing; Information Theory; Codes, Fields and Curves; Abstract Algebra; Applied Linear Algebra; Advanced VLSI Design; Advanced VLSI Architecture; VLSI Digital Signal Processing; Computer Architecture; Algorithms and Data Structures; GPU Programming; Applied Parallel Computing; Advanced Optimization Techniques; Applied Machine Learning.